CLAIMS

1. An embeddable flash memory system, comprising a non-volatile memory for non-volatile storage of code, data, and bit-streams for embedded FPGA configurations, the system integrated into a single chip together with a microprocessor and having a modular array structure comprising a plurality of memory blocks, wherein a power block comprising charge pumps is shared among different flash memory modules through a PMA arbiter.

2. The embeddable flash memory system of claim 1, comprising three different access ports, each for a specific function:

a code port CP optimized for random access time and the application system;

a data port DP for access to modify application data; and,

an FPGA port FP offering a serial access for a fast download of bit streams for an embedded FPGA configurations.

3. The embeddable flash memory system of claim 1 wherein said PMA arbiter block includes an order block configured to order requests for the memory blocks following these rules:

status of the request (already active or new request);

priority information.

4. The embeddable flash memory system of claim 3, comprising a switch block managing the requests of the memory blocks based on the output of said order block; a request decoder block configured to enable the required high voltage resources while a corresponding pump driver block manages a power down/stand-by timeout and limits requests for each resource to a maximum allowed.

5. The embeddable flash memory system of claim 1 wherein said code port CP comprises four configuration registers defining its addressable memory space: two at the application level, and two at the flash memory modules level.

6. The embeddable flash memory system of claim 1 wherein said second data port DP manages application data stored in the memory blocks using an SRAM page buffer configured to enable the application to exchange data in burst mode at maximum speed to increase performance during write operation.

7. The embeddable flash memory system of claim 5 wherein said third FP port comprises four configuration registers replicating information stored in said code port CP that is used to write e-FPGA configurations data.

8. The embeddable flash memory system of claim 1 wherein said FP port uses a chip select to access addressable memory space and a burst enable to enable burst serial access.

9. The embeddable flash memory system of claim 1 wherein a DFT block is provided and connected to all relevant internal signals for first internal testing and then all internally generated voltages and currents system testability; said DFT block coupled to an external high voltage power supply, and two analog IO pads configured to provide access from external test equipment.

10. A memory system, comprising:

a memory module, the memory module comprising a non-volatile memory block; a power block; and a power management arbiter coupling the power block to the non-volatile memory block, the arbiter configured to provide charge pump sharing among flash memory modules in the non-volatile memory block from a single charge pump in the power block.

11. The system of claim 10 wherein the non-volatile memory block comprises a plurality of flash memory modules having a multi-bank configuration.

12. The system of claim 10 wherein the power management arbiter comprises an order block configured to order requests for the memory modules in the non-volatile memory block.

13. The system of claim 10 wherein the power management arbiter further comprises a programming circuit having a multiplexer receiving as an input a voltage from a voltage regulator and having an output coupled to a row decoder for providing a read voltage to memory matrix rows, and a program switch coupling an output from the charge pump to a column decoder for biasing memory matrix columns in the memory modules with a voltage generated by the charge pump.

14. The system of claim 10, further comprising a testing block coupled to the power block and the power management arbiter and configured to provide external access for testability.

15. The system of claim 14 wherein the microprocessor is configured to test the memory system, and wherein the testing block further comprises an analog-to-digital converter for enabling access by external analog test equipment.

16. The system of claim 10, further comprising a code port coupled to the memory module and configured to manage application code stored in the memory module; a data port coupled to the memory module and configured to manage application data stored in the memory module; and a floating programmable gate array port coupled to the memory module and configured to manage embedded floating programmable gate array configuration data stored in the memory module.

17. A memory system, comprising a plurality of non-volatile flash memory blocks;

a power block comprising a plurality of charge pumps;

a power management arbiter coupled to the power block and to the non-volatile flash memory blocks, the power management arbiter comprising a programming circuit configured to couple the charge pumps to the memory blocks and an order block configured to order power requests for the memory blocks;

a crossbar coupled to the memory blocks, power block, and power management arbiter;

a code port coupled to the crossbar and configured to optimize random access time and to manage application code stored in the memory blocks;

a data port coupled to the crossbar and configured to provide access to and modify application data stored in the memory blocks;

a floating programmable gate array port coupled to the crossbar and configured to provide serial access for download of bit streams of embedded floating programmable gate array configurations stored in the memory modules; and

a microprocessor coupled to the crossbar and configured to provide data management and memory system testing.

18. The system of claim 17, further comprising a testing block coupled to the power block and the power management arbiter and configured to provide access to the memory system for testing, the testing block comprising an analog-to-digital converter having an analog input configured to communicate with external analog testing equipment.

19. The system of claim 18 wherein the order block is configured to order requests for the memory blocks in accordance with the following rules:

status of the request (already active or new request); and

priority information.

20. The system of claim 19 wherein the power management arbiter comprises a switch block coupled to an output of the order block and configured to manage requests for the memory blocks in response to output of the order block; and a request decoder block configured to enable the charge pumps; and a pump driver block configured to manage power down/stand-by timeout and to limit requests for each charge pump to a maximum allowed number of requests.